TED (15/19)3131
(Revision – 2015/19)

A25 - 6679

Reg. No……
Signature ……

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, APRIL - 2025

COMPUTER ARCHITECTURE

[Maximum Marks: **100**] [Time: **3** Hours]

PART-A

[Maximum Marks: **10**]

I. (Answer ***all*** questions in one or two sentences. Each question carries ***2*** marks)

1. List Advanced DRAM.
2. Define the terms inter sector gap, inter track gap.
3. Recall the term PSW.
4. Define register.
5. Define micro instruction . (5 x 2 = 10)

PART-B

[Maximum Marks: **30**]

II. (Answer ***any five*** of the following questions. Each question carries ***6*** marks)

1. Write a short note on instruction cycle with a neat diagram.
2. List and explain cache memory principles.
3. Explain step by step the procedure of transferring data using DMA.
4. Compare programmed I/O and interrupt driven I/O.
5. Define the term hazard. Explain control hazard during pipeline.
6. Write the symbolic form of interrupt cycle and explain.
7. What is the role of registers in CPU? (5 x 6 = 30)

PART-C

[Maximum Marks: **60**]

(Answer ***one*** full question from each Unit. Each full question carries **15** marks)

UNIT – I

III. a. Draw and explain Von Neumann architecture. (7)

b. List and explain the things you must consider during the cache design. (8)

OR

IV. a. List and explain the elements that you should consider during the bus design. (10)

b. List and explain types of ROM. (5)

UNIT – II

V. a. Write a report on RAID and its all 7 levels. (10)

b. Compare RAID levels. (5)

OR

VI. a. Explain the role of I/O module when cpu want to take some input from keyboard. (10)

b. Classify external devices and give example for each. (5)

UNIT- III

VII. a. Explain the concept of pipeline with an example. (9)

b. Explain data flow in an instruction cycle with a neat diagram. (6)

OR

VIII. a. Describe the Internal structure of CPU with a neat diagram. (8)

b. Write a short note on Register organizations. (7)

UNIT - IV

IX. a. Explain Flynns classification of parallel processing system. (10)

b. Draw and explain the block diagram of control unit. (5)

OR

X. a. Draw and explain the block diagram of Micro programmed controller. (9)

b. Explain Hardwired micro controller. (6)

****