TED (15/19) - 3212
(REVISION-2015/19)

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Reg.No……
Signature…….

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER - 2024

DIGITAL CIRCUITS

(Maximum Marks:100) (Time: 3 Hours)

PART - A

(Maximum Marks : 10)

Marks

I. Answer **all** the questions in one or two sentences. Each question carries 2 marks.

1. List the four types of number system.
2. Draw the symbol of NOR gate with its truth table.
3. Define Fan-out & Fan-In.
4. Define asynchronous counter.
5. Write the name of any two A/D ICs. (5 x 2 = 10)

PART - B

(Maximum Marks: 30)

II Answer ***any five*** questions from the following. Each question carries 6 marks.

1. Minimize the following function using K map $F(a,b,c)=\sum m\,(1,2,5,6)$
2. Explain the procedure to convert octal to decimal number system and convert the octal code $(140)_8$ into decimal.
3. With neat diagram describe the operation of 4 to 1 Multiplexer.
4. Draw the circuit and explain the operation of TTL NAND gate.
5. Draw the circuit diagram of asynchronous decade counter and give its truth table.
6. List any six applications of flip flop.
7. Compare ROM and RAM. (5 x 6 = 30)

PART – C

(Maximum Marks: 60)

(Answer ***one full*** question from each unit. Each full question carries 15 marks.)

UNIT - I

III (a) Write a short notes of Excess 3 code and Gray code. (4)

(b) Simplify the expression $\overline{\overline{A + B\bar{C}} + D.\overline{(E + \bar{F})}}$ using De-Morgan's theorem (7)

(c) State associate law of addition and associate law of multiplication. (4)

OR

IV (a) Implement AND, OR. and EX-OR gates using NAND gates only. (6)

(b) Substract using 2's complement method.

(i) $(1111)_2 - (1010)_2$ (ii) $(1000)_2 - (1010)_2$ (4)

(c) Simplify the logic expression [AB'(C+BD)+A'B']C using linear algebra. (5)

UNIT – II

V (a) Implement the Boolean function F = ($\bar{A}$ +B+C).(A+B).D using only NOR gate. (7)

(b) Explain the operation of 4 bit Look ahead carry adder with block diagram. (8)

OR

VI (a) Describe the operation of decimal to BCD encoder. (8)

(b) Describe the operation of 4 bit binary parallel adder. (7)

UNIT – III

VII (a) Explain the operation of Parallel-in Serial-out shift register with neat sketch. (7)

(b) Draw the logic diagram and explain the mod-12 asynchronous counter using JK flip flop. (8)

OR

VIII (a) Draw and explain the operation of JK flip flop with its truth table. (7)

(b) Describe the operation of up/down asynchronous counter. (8)

UNIT – IV

IX (a) Explain the operation of binary weighted D/A converter. (7)

(b) Explain the operation of successive approximation type A/D converter. (8)

OR

X (a) Briefly explain sensitivity and resolution of a digital meter. (6)

(b) Explain the operation of R-2R ladder type DAC converter with neat sketch. (9)

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