TED (15/19)3133
(Revision – 2015/19)

A23-08250

Reg. No……
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, APRIL – 2023

DIGITAL COMPUTER PRINCIPLES

[Maximum Marks: **100**] [Time: **3** Hours]

PART-A

[Maximum Marks: **10**]

I. (Answer ***all*** questions in one or two sentences. Each question carries ***2*** marks)

1. Find 2's complement of 10110010.
2. What is K-map?
3. What are flipflops? Give two examples.
4. Name any one error detection & correction code.
5. What is PAL? (5 x 2 = 10)

PART-B

[Maximum Marks: **30**]

II. (Answer ***any five*** of the following questions. Each question carries ***6*** marks)

1. Realize OR, EX-OR gates using NAND gates.
2. Reduce the expression F = A +B[AC +(B+C')D].
3. Convert Y =A+ B'C into standard. SOP form.
4. Design and implement a 4-bit binary to gray codeconverter.
5. Differentiate synchronous and asynchronous sequential circuits.
6. Describe the circuit of a D-flipflop with a neat diagram.
7. Explain about memory decoding. (5 x 6 = 30)

PART-C

[Maximum Marks: **60**]

(Answer ***one*** full question from each Unit. Each full question carries **15** marks)

UNIT – I

III. a. Explain basic gates with logic diagram and truth table. (9)

b. State and prove De-Morgan's Theorems. (6)

OR

IV. a. Convert i) $(4F7.A8)_{16}$ to Octal (ii) $(10110.0101)_2$ to hexadecimal
iii) $(163.875)_{10}$ to binary. (9)

b. Draw logic symbols and truth table of universal gates and explain. (6)

UNIT – II

V. a. Define maxterm. Expand A **(B'+A) B** to standard POS form. (8)

b. Design the working of a 4 x 1 multiplexer with neat sketch. (7)

OR

VI. a. Minimize **F (A, B, C, D)** = Σm **(1, 4, 7, 10, 13)** + **d (5, 14, 15)** using K-map. (8)

b. Draw and explain the working of a 4-bit binary adder. (7)

UNIT- III

VII. Explain the basic operations of shift registers with neat sketch. (15)

OR

VIII. a. Explain the working of a J-K flipflop with diagram and truth table. (8)

b. Design a 4-bit ring counter. (7)

UNIT - IV

IX. a. Realize the following functions using PLA.

Fl = AB'+ AC+A'BC'

F2 = (AC+ BC)' (9)

b. List and explain various DAC specifications. (6)

OR

X. a. Explain R-2R ladder DAC with diagram. (8)

b. Explain the working of counter ramp type ADC with diagram. (7)

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