TED (15/19) – 3212
(Revision – 2015/19)

A23 -06335

Reg.No……..
Signature……...

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE , APRIL – 2023

DIGITAL CIRCUITS

(Maximum Marks : 100) (Time : 3 hours)

PART – A
(Maximum Marks : 10)

Marks

I. Answer **all** questions in one or two sentences. Each question carries 2 marks.

1. Define minterm..
2. Define Speed power product.
3. What is meant by modulus of a counter?
4. List any two applications of shift register.
5. Define a byte and a nibble.

(5x2=10)

PART – B
(Maximum Marks : 30)

II. Answer any **five** of the following questions. Each question carries 6 marks.

1. State and prove De Morgan's theorem.
2. Explain the working of a 4 to 1 Multiplexer.
3. Explain the working of a TTL inverter with the help of circuit diagram.
4. Compare synchronous and asynchronous counter.
5. Explain briefly serial in serial out shift registers.
6. Explain the operation of single slope Analog to Digital converter.
7. Compare ROM and RAM.

(5x6=30)

PART – C
(Maximum Marks : 60)
(Answer **one full** question from each unit. Each full question carries 15 marks)

UNIT – I

III. (a) Convert the following as directed.

(i) $(63.875)_{10}$ to ($)_2$ (ii) $(10101.101)_2$ to ($)_{10}$

(iii) $(378.4375)_{10}$ to ($)_8$ (iv) $(4057.06)_8$ to ($)_{10}$ (4x2=8)

(b) Simplify the following expression using Karnaugh map

$f(A,B,C,D)= \Sigma m(0,1,4,6,7,15) + \Sigma d(3,5,13)$ (7)

OR

IV. (a) Perform the following binary arithmetic.

(i) 1101.101 + 111.011 (ii) 1010.010 – 111.111

(iii) 1101 x 1.10 (iv) 1100 ÷ 100 (4x2=8)

(b) Reduce the following expression using Boolean algebra:

$F=\overline{\bar{A}B + A\bar{C}} + \bar{A}\bar{B}C$. (7)

UNIT – II

V. (a) Describe the operation of decimal to BCD encoder. (8)

(b) Explain the operation of a 4 bit parallel binary adder. (7)

OR

VI. (a) What is full adder? Write its truth table and realise it using NAND gates alone. (8)

(b) Explain the working of TTL NAND gate. (7)

UNIT –III

VII. (a) With help of truth table and circuit diagram, explain the working of Master slave pulse triggered JK flipflop. (8)

(b) Draw and explain a decade asynchronous counter using JK flip flop. (7)

OR

VIII. (a) Explain the working of a parallel in serial out shift register. (8)

(b) Explain the operation of an edge triggered SR flipflop with the help of circuit diagram and truth table. (7)

UNIT – IV

IX. (a) Explain the operation of R-2R Digital to Analog converter. (8)

(b) Explain the operation of Successive approximation Analog to Digital converter. (7)

OR

X. (a) Briefly explain different types of ROM. (8)

(b) Explain the working of Weighted resistor Digital to Analog converter. (7)

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