TED (15/19) -3133
(Revision- 2015/19)

N21-09783

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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/
COMMERCIAL PRACTICE –NOVEMBER -2021.

DIGITAL COMPUTER PRINCIPLES

(Maximum Marks : 75) [Time : 2.15 hours]

PART–A

Marks

I. Answer **any three** questions in one or two sentences. Each question carries 2 marks.

1. Write 2 examples for non-weighted code.
2. Define an encoder.
3. List two types of sequential circuits based on timing of signals.
4. Define the term resolution.
5. List different types of RAMs. (3x2=6)

PART - B

II Answer **any four** of the following questions . Each question carries 6 marks.

1. Implement an X-OR gate and OR gate using NAND gate.
2. Write short notes on.
   a) BCD code b) XS-3 code
3. Convert the following SOP into standard SOP.
   $Y=A+\overline{B}C$
4. Describe the working of R-S flip flop using NAND gate.
5. Design and implement a half subtractor circuit.
6. Differentiate between sequential and combinational circuit.
7. Describe the need of DAC and ADC in digital systems.

(4x6 =24)

PART - C

(Answer **any of the three units** from the following. Each full question carries 15 marks)

UNIT I

III (a) State De Morgan's theorem. Using it reduce the following expressions.

1. $\overline{\bar{A}\bar{B}+\bar{A}+A\bar{B}}$ 2. $\overline{(A+\bar{B})(C+\bar{D})}$ (8)

(b) State the advantages of performing subtraction by complement method.

Perform 2's compliment subtraction for the following binary numbers.

1. 110000 - 10101 2. 1001 – 101000 (7)

OR

IV (a) Perform the following conversions.

1. $(F5A\text{-}16)_{16}$ to binary 2. $(10110.0101)_2$ to hexadecimal.

3. $(32.24)_8$ to decimal 4. $(895)_{10}$ to octal (8)

(b) Draw the logic symbol and truth table for universal gates. (7)

UNIT- II

V (a) Design and implement a full adder circuit. (8)

(b) Define K-map. List the merits and demerits of K-map. (7)

OR

VI (a) Describe the working of a four input multiplexer. (8)

(b) Minimize the following expression using K-map.
$F(W,X,Y,Z) = \Sigma(1,4,7,10,13) + \Sigma d(5,14,15)$ (7)

UNIT- III

VII (a) Explain the working of a J K flip flop with a truth table and diagram. (8)

(b) Describe the working of a 3 bit serial in serial out shift register. (7)

OR

VIII (a) Design an asynchronous mod-6 counter using J K flip flop. (8)

(b) Draw the circuit diagram and truth table of a 4 bit ring counter. (7)

UNIT – IV

IX (a) Describe the working of a R-2R ladder type DAC. (8)

(b) Explain different types of ROMs. (7)

OR

X (a) Develop a programming table for PAL for Boolean functions.

$W = AB\bar{C} + \bar{A}\bar{B}C\bar{D}$

$X = A + BCD$

$Y = \bar{A}B + CD + \bar{B}\bar{D}$

$Z = AB\bar{C} + \bar{A}\bar{B}C\bar{D} + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$ (8)

(b) Using appropriate example explain error correction and detection using hamming code. (7)

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