DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/
COMMERCIAL PRACTICE –NOVEMBER -2021.

DIGITAL CIRCUITS

(Maximum Marks : 75)   [Time : 2.15 hours]

PART–A

Marks

I. Answer **any three** questions in one or two sentences. Each question carries 2 marks.

1. Convert $(367.52)_8$ to binary.

2. Define fan in of a logic gate.

3. List the asynchronous inputs to a flip flop.

4. Define sensitivity of a digital meter.

5. Define the modulus of a counter.   (3x2=6)

PART - B

II   Answer **any four** of the following questions . Each question carries 6 marks.

1. State Demorgan's theorems.

2. Explain the operation of a Full adder.

3. Illustrate the operation of a edge triggered J-K flip flop.

4. Compare RAM and ROM.

5. Simplify $f = \overline{(A+\overline{BC})}.(A\overline{B}+ABC)$ using Boolean laws.

6. Implement EX-OR gate using NAND gate.

7. Draw the logic diagram of a serial in parallel out shift register.

(4x6 =24)

PART - C

(Answer **any of the three units** from the following. Each full question carries 15 marks)

UNIT I

III (a) Solve the following (i) $(110101.101010)_2 = (-----)_8$ (ii) Multiply $(1101)_2$ by $(110)_2$. (6)

(b) Reduce the expression $F = \Sigma m\ (0, 1, 2, 3, 6, 7, 13, 15)$ using K –map. (9)

OR

IV (a) Solve the following (i) Divide $(101101)_2$ by $(110)_2$ (ii) $(3A9E.B0D)_{16} = (-----)_2$. (6)

(b) Reduce the expression $F = \prod M(0,1,2,3,4,10,11,15)$ using K-map.
(9)

UNIT- II

V (a) Explain the operation of a TTL NAND gate. (9)

(b) Illustrate the operation of a 4X1 Multiplexer. (6)

OR

VI (a) Explain the operation of a BCD-Decimal decoder. (9)

(b) Illustrate the operation of a one bit comparator. (6)

UNIT- III

VII (a) Design a decade asynchronous counter. (9)

(b) Draw the circuit of a parallel in serial out shift register. (6)

OR

VIII (a) Design a 4 bit synchronous counter. (9)

(b) Compare synchronous counter and asynchronous counter. (6)

UNIT – IV

IX (a) Explain the operation of a single slope A/D Converter. (8)

(b) Describe the working of a binary weighted converter. (7)

OR

X (a) Explain the operation of Successive approximation A/D converter. (8)

(b) Describe the working of a R-2R D/A converter. (7)

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