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(Revision – 2015/19)

N21 – 07115

Reg. No……
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER – 2021

DIGITAL ELECTRONICS

[Maximum Marks: **75**] [Time: **2.15** Hours]

PART-A

(Answer ***any three*** questions in one or two sentences. Each question carries ***2*** marks)

I. 1. Define BCD code and give example for a BCD number.

2. Differentiate between combinational and sequential logic circuits.

3. State the race around condition in JK flip flop

4. Define settling time of DACs.

5. Write the 1's complement and 2's complement of the binary number 110010. (3 x 2 = 6)

PART-B

(Answer ***any four*** of the following questions. Each question carries ***6*** marks)

II. 1. Simplify the expression $AB + \overline{AC} + A\bar{B}C(AB + C)$?

2. Explain the circuit of TTL inverter.

3. Design a half subtractor circuit.

4. Explain the working of Johnson counter with circuit diagram?

5. Draw the SR flip flop using NAND gate and explain its characteristic table.

6. Differentiate between synchronous and asynchronous counters.

7. Explain weighted resistor DAC? (4 x 6 = 24)

PART-C

(Answer ***any of the three units*** from the following. Each full question carries ***15*** marks)

UNIT – I

III. (a) Do the following

(1) 101001-110 (2) 1001011 ÷ 101

(3) $3024)_D=(\quad)_H$ (4) $91AE)_H=(\quad)_B$ (12)

(b) Explain why binary number system is preferred in digital electronic systems. (3)

OR

IV. (a) Simplify using K- map and realize

$F(A,B,C,D) = \Sigma(0,1,2,3,4,7,8,10) + d(5,6,9,11,12,14)$ (12)

(b) Give the need for simplifying Boolean expression (3)

UNIT – II

V. (a) Explain the design and operation of 4x1 Multiplexer. (8)

(b) Design a full adder circuit. (7)

OR

VI. (a) Explain code converters and design a 4-bit binary to gray code converter. (10)

(b) Compare the features of TTL, ECL and CMOS logic families (5)

UNIT – III

VII. (a) Explain JK flip-flop using NAND with the help of truth table. (8)

(b) Differentiate between right shift and left shift registers with logic diagram. (7)

OR

VIII. (a) Illustrate and explain the working of SISO and SIPO shift registers. (8)

(b) Explain the working of ring counter and give its applications. (7)

UNIT – IV

IX. (a) Implement mod-10 asynchronous counter using JK flip flop. (8)

(b) Describe the working of Successive approximation type ADC. (7)

OR

X. (a) Design 3 bit up-down counter using JK flip flop. (8)

(b) Explain R-2R ladder type DAC with circuit diagram (7)

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