TED (15) 3131 | A21-08254 | Reg.No.....

(Revision-2015/19) | Signature.....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, APRIL-2021

COMPUTER ARCHITECTURE

[Maximum marks: 75] (Time: 2.15 Hours)

PART – A

I (Answer any ***three*** questions in one or two sentences. Each question carries 2 marks)

1. Mention the purpose of bus.
2. Define seek time.
3. List the stages of an Instruction Cycle.
4. State micro program.
5. Define Parallel processing (3 x 2 = 6)

PART – B

II (Answer any ***four*** of the following questions. Each question carries 6 marks)

1. Describe the Von-Neumann machine with neat diagram.
2. Compare static RAM and dynamic RAM.
3. Write the physical characteristics of Disk systems.
4. Write short note on DMA.
5. Explain instruction pipelining.
6. Explain Control and status registers.
7. Draw the block diagram of control unit and write the major tasks. (4 x 6= 24)

PART – C

(Answer ***any of the three units*** from the following. Each full question carries 15 marks)

UNIT –I

III. (a) Explain typical memory hierarchy with neat diagram (8)

(b) Describe advanced DRAM types. (7)

OR

IV. (a) Briefly describe the elements of bus design. (8)

(b) Discuss characteristics of computer memory system. (7)

UNIT-II

V. (a) Draw I/O module structure and mention the major functions (8)

(b) Discuss interrupt driven I/O (7)

OR

VI. Discuss the different RAID Levels. (15)

UNIT-III

VII.(a) Explain pipeline hazards. (8)

(b) Draw and explain the instruction cycle state diagram (7)

OR

VIII.(a) Describe user visible registers. (8)

(b) Discuss internal structure of CPU with a neat diagram (7)

UNIT-IV

IX. (a) Draw and explain micro programmed control unit. (8)

(b) Describe the micro operations involved in fetch cycle (7)

OR

X. Discuss Flynn's classification of parallel processing systems. (15)

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