

**DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/
COMMERCIAL PRACTICE, NOVEMBER - 2023**

DIGITAL CIRCUITS

[Maximum marks: 100]

[Time: 3 Hours]

PART – A

Maximum marks: 10

I (Answer *all* the questions in one or two sentences. Each question carries **2** marks)

1. List any two unweighted codes.
2. Define fan-in and fan-out.
3. Define glitch.
4. List the asynchronous inputs to flip-flops.
5. Define resolution of digital meter. (5 x 2 = 10)

PART – B

Maximum marks: 30

II (Answer any *five* of the following questions. Each question carries **6** marks)

1. Subtract using 2's complement method.
(i) $1101_2 - 0101_2$ (ii) $10011_2 - 11001_2$ (iii) $10110_2 - 110_2$
2. Convert the following to decimal number system.
(i) 357_8 (ii) $9B47_{16}$ (iii) 110011_2
3. Explain the operation of TTL NOT gate.
4. Outline the drawback of S-R flip-flop and explain how it is eliminated.
5. Describe serial in parallel out shift register.
6. Compare ROM and RAM.
7. Describe the working of single slope A/D converter. (5 x 6 = 30)

PART – C

Maximum marks: 60

(Answer *one full* question from each unit. Each full question carries **15** marks)

UNIT – I

III. (a) Simplify the following expressions using Boolean laws.

- (i) $\bar{A}BC + A\bar{B}C + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$ (ii) $A + AB + ABC + ABCD$
(iii) $AC + [\bar{B} + A(B + \bar{C})]$ (9)

(b) Convert the following numbers.

(i) $1100111011_2 = (\dots)_{16}$ (ii) $142_8 = (\dots)_2$ (iii) $11001_2 = (\dots)_{\text{gray}}$ (6)

OR

IV. (a) Simplify using K – map $f = \sum m(0,1,2,7,8,9,10) + d(6,12,13)$ (9)

(b) Perform: (i) $11001_2 + 10111_2$ (ii) $1010_2 - 101_2$ (iii) $1011_2 \times 101_2$ (6)

UNIT-II

V. (a) Explain the operation of TTL NAND gate. (8)

(b) Explain the implementation of basic gates using universal gate NAND. (7)

OR

VI. (a) Explain the operation of 4 x 1 multiplexer. (8)

(b) Describe the operation of full adder with logic circuit. (7)

UNIT-III

VII. (a) Describe the working of serial in serial out shift register. (7)

(b) Design a synchronous decade counter. (8)

OR

VIII. (a) Describe the working of Master-Slave J-K flip flop. (7)

(b) Design a four bit asynchronous counter. (8)

UNIT-IV

IX. (a) Explain the working of successive approximation Analog to Digital converter. (8)

(b) Describe the working of Binary weighted Digital to Analog converter. (7)

OR

X. (a) Explain the various RAMs. (8)

(b) Describe the working of R – 2R Digital to Analog converter. (7)
