TED (21)3081
(Revision – 2021)

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Reg. No……
Signature …….

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER – 2023

DIGITAL CIRCUITS AND SYSTEMS

[Maximum Marks: **75**] [Time: **3** Hours]

PART-A

I. Answer *all* the following questions in one word or one sentence. Each question carries *'one'* mark.

(9 x 1 = 9 Marks)

		Module Outcome	Cognitive level
1.	List any one alphanumeric code.	M1.01	R
2.	 Find the output Y, if A=1 and B=0	M1.02	U
3.	Define a decoder.	M2.04	R
4.	Number of select switch needed for 4:1 multiplexer is	M2.03	A
5.	Output of a adder circuit is …… and……..	M2.01	R
6.	Define modulus of a counter.	M3.06	R
7.	List out the application of shift register.	M3.04	R
8.	Asynchronous inputs of a flip flop are ……. and …….	M3.03	U
9.	Define step size of a DAC.	M4.04	R

PART-B

II. Answer any *eight* questions from the following. Each question carries *'three'* marks.

(8 x 3 = 24 Marks)

		Module Outcome	Cognitive level
1.	Do the following a)11001100_2 + 11011010_2 b)11010_2 - 10000_2	M1.01	U
2.	Draw the symbol and truth table of 3 input NOR gate.	M1.02	R
3.	State DeMorgan's Theorem.	M1.03	R
4.	Implement F= (A+B)(A+$\bar{B}$') using basic gates.	M1.03	A
5.	Draw the truth table and logic diagram of half subtractor.	M2.02	U
6.	Differentiate between synchronous and asynchronous sequential circuit.	M3.01	U
7.	Draw the logic symbol and Truth table of D-Flip flop.	M3.02	U
8.	Mention the methods of eliminating race around condition in JK flip Flop.	M3.03	U
9.	Draw the circuit of a 3 bit asynchronous updown counter.	M3.08	U
10.	Mention the advantages of R-2R ladder type DAC.	M4.01	R

PART-C

Answer all questions from the following. Each question carries *'seven'* marks

(6 x 7 = 42 Marks)

		Module Outcome	Cognitive level
III.	Reduce the 4- variable expression F(A, B,C,D)=Σ m (1,3,6,9,l l,14) + Σ d(7,15) using K map.	M1.03	U
	OR		
IV.	Implement the following function using NAND -NAND Logic A'B' +A'C +B'C	M1.02	U
V.	Design a full adder circuit, Explain its operation, implement it using basic gates.	M2.01	A
	OR		
VI.	Design BCD to Decimal Decoder with its truth table and logical diagram.	M2.04	A
VII.	Design and Implement a 4 to 1 multiplexer using logic gates.	M2.03	A
	OR		
VIII.	Describe the working of 4 bit Parallel adder with block diagram.	M2.01	U
IX.	Explain with the aid of truth table and logic diagram the working of Master -Slave JK Flip Flop.	M3.03	U
	OR		
X.	Explain the working of Serial -In Serial out shift register using truth table and timing diagram.	M3.04	U
XI.	Draw a 4-bit ring counter and explain its operation.	M3.05	U
	OR		
XII.	Describe an asynchronous mod-10 counter.	M3.06	U
XIII.	Describe the working of binary weighted resistor DAC with necessary diagram.	M4.01	U
	OR		
XIV.	Describe the working of successive approximation type ADC using relevant diagram.	M4.03	U

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