TED (15/19) – 3131
(Revision – 2015/19)

N22 - 06182

Reg.No……..
Signature……...

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE – NOVEMBER – 2022

COMPUTER ARCHITECTURE

(Maximum Marks : 100) (Time : 3 hours)

PART – A
(Maximum Marks : 10)

Marks

I. Answer **all** questions in one or two sentences. Each question carries 2 marks.

1. Define PC and IR.
2. What is DMA?
3. What is PSW?
4. Define micro operation.
5. Define system bus. (5x2=10)

PART – B
(Maximum Marks : 30)

II. Answer any **five** of the following questions. Each question carries 6 marks.

1. Write down the sequence of micro operations for ADD R1,X.
2. Explain the principles of cache memory.
3. Explain about DVD.
4. Explain the data flow for indirect cycle.
5. Explain the hardwired implementation of control unit.
6. Explain about interrupts.
7. Explain magnetic read and write mechanism. (5x6=30)

PART – C
(Maximum Marks : 60)
(Answer **one full** question from each unit. Each full question carries 15 marks)

UNIT – I

III. (a) Explain the instruction cycle state diagram. (9)

(b) Explain the Dynamic RAM structure with a neat sketch. (6)

OR

IV. (a) Explain the top level view of computer components. (9)

(b) Explain the memory hierarchy. (6)

UNIT – II

V. (a) Explain the physical characteristics of disk system. (9)

(b) Explain the block diagram of external device. (6)

OR

VI. (a) Explain interrupt driven I/O. (6)

(b) Explain different RAID levels with neat sketch. (9)

UNIT –III

VII. (a) Explain user visible registers. (6)

(b) Explain instruction pipelining. (9)

OR

VIII. (a) Explain the internal structure of the CPU. (9)

(b) Explain the data flow for interrupt cycle. (6)

UNIT – IV

IX. (a) Explain micro programmed control unit. (9)

(b) Explain the micro operations for fetch cycle. (6)

OR

X. (a) Explain different multiple processor organization with diagrams of each. (10)

(b) Explain the block diagram of a control unit. (5)

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