TED (21) 3081
(Revision – 2021)

**N22-2110220059 A**

Reg. No……
Signature ……

# DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER – 2022

## DIGITAL CIRCUITS & SYSTEMS

[Maximum Marks: **75**] [Time: **3** Hours]

### PART-A

**I. Answer *all* the following questions in one word or one sentence. Each question carries *'one'* mark.**

**(9 x 1 = 9 Marks)**

| | | Module Outcome | Cognitive level |
|---|---|---|---|
| 1. | Define Radix of a number system. | M1.01 | R |
| 2. | Write the truth table of a NOR gate. | M1.02 | R |
| 3. | Define Decoder. | M2.04 | R |
| 4. | Write any two applications of De-Multiplexer. | M2.03 | R |
| 5. | Name any two flip flop's used in digital circuits. | M3.02 | R |
| 6. | Define modulus of a counter. | M3.06 | R |
| 7. | Define up down counter. | M3.08 | R |
| 8. | Write the disadvantages of Binary resistor DAC. | M4.01 | U |
| 9. | List any two ADC. | M4.04 | R |

### PART-B

**II. Answer any *eight* questions from the following. Each question carries *'three'* marks.**

**(8 x 3 = 24 Marks)**

| | | Module Outcome | Cognitive level |
|---|---|---|---|
| 1. | Convert $215_{(10)}$ to binary, Octal and Hexadecimal. | M1.01 | A |
| 2. | State De-Morgan's Theorem. | M1.03 | R |
| 3. | Draw the logic diagram of an Ex OR gate using NOR gates. | M1.02 | R |
| 4. | Draw the logic diagram of 4:1 Multiplexer. | M2.03 | U |
| 5. | Design a Half Subtractor circuit using NAND gates. | M2.02 | A |
| 6. | Design a 3 bit encoder. | M2.04 | A |
| 7. | Compare Asynchronous and Synchronous sequential circuits. | M3.01 | U |
| 8. | Explain the working of Serial In Serial Out Shift register. | M3.04 | U |
| 9. | Draw the circuit diagram of a Ring counter. | M3.05 | U |
| 10. | Define Resolution and Offset voltage of DAC. | M4.04 | U |

## PART-C

**Answer all questions. Each question carries *'seven'* marks.**

**(6 x 7 = 42 Marks)**

| | | Module Outcome | Cognitive level |
|---|---|---|---|
| III. | Solve the following<br>a. 11011 – 10110 (using 2's complement method)<br>b. 1001-1100 (using 1's (complement method)<br>c. 101111÷ 101<br>d. 1110 x 101 | M1.01 | A |
| | **OR** | | |
| IV. | Minimize the expression f=Σm (1,2,6,7,8,13,14,15)+d (3,5,12) | M1.03 | A |
| V. | Describe a Full Adder using basic gates. | M2.02 | U |
| | **OR** | | |
| VI. | Describe BCD to Decimal decoder. | M2.04 | U |
| VII. | Explain the working of Parallel binary adder with circuit diagram. | M2.01 | U |
| | **OR** | | |
| VIII. | Design a 3 bit Binary to Gray code convertor using Basic gates. | M2.06 | A |
| IX. | Describe the working of S R flip flop using NAND gates. | M3.02 | U |
| | **OR** | | |
| X. | Design mod-8 Synchronous Counter. | M3.07 | U |
| XI. | Draw the circuit diagram Truth table and Timing diagram of 3bit Johnson Counter. | M3.05 | U |
| | **OR** | | |
| XII. | Describe 3 bit up-down Counter. | M3.08 | U |
| XIII. | Describe the working of R-2R Ladder type DAC. | M4.02 | U |
| | **OR** | | |
| XIV. | Describe the working of Successive Approximation type ADC. | M4.03 | U |

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