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(Revision – 2015/19)

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Reg. No……
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, APRIL – 2021

DIGITAL COMPUTER PRINCIPLES

[Maximum Marks: 75] [Time: 2.15 Hours]

PART-A

(Answer ***any three*** questions in one or two sentences. Each question carries 2 marks)

I.

1. Name any one weighted and unweighted code in digital system.
2. Write any two error detecting and correcting codes.
3. Differentiate between SOP and POS in digital systems.
4. Write any two main types of counters.
5. Define a PLA. (3×2=6)

PART-B

(Answer ***any four*** of the following questions. Each question carries *6* marks)

II.

1. Convert (10110) gray= (-----) binary, 9A5C= (----) octal, (126) decimal (----) Binary.
2. Draw the logic symbol and truth tables of NOT, AND and OR gates.
3. Explain the working of half adder with logic diagram and truth table.
4. Explain the universal property of NAND gate with logic diagram.
5. Explain the working of clocked RS flip-flop with logic diagram and truth table.
6. Draw a ring counter using D flip flop with a state table.
7. Briefly explain RAM and ROM.

(4×6=24)

PART-C

(Answer ***any of the three units*** from the following. Each full question carries 15 marks)

UNIT-I

III. (a) State and prove Demorgans theorems. (8)

(b) Simplify the Boolean equation Y=A'B'C'+A'BC'+AB'C'+ABC'. (7)

OR

IV. (a) Explain the following codes Binary, BCD, ASCII, Octal. (10)

(b) Subtract 001110 from 110101 using 2s complement method. (5)

UNIT – II

V. (a) Simplify the following using K-map, F (A,B,C,D)=Σm(1,5,6,10,13,14)+d(2,9). (10)

(b) Design an Ex_OR gate only using NAND gates. (5)

OR

VI. (a) Design and implement 8 to 1 multiplexer with logic diagram and truth table. (8)

(b) Design and implement a full adder with logic diagram and truth table (7)

UNIT – III

VII. (a) Explain the working of JK flip-flop with logic diagram and truth table. (8)

(b) Draw the logic diagram and state table of a 4-bit Johnson counter. (7)

OR

VIII. (a) Name different types of registers. Explain any two. (8)

(b) Draw the logic diagram and state table of a 3-bit ripple up counter. (7)

UNIT – IV

IX. (a) Explain the PAL with a suitable diagram. (8)

(b) Explain the working of an R-2R Ladder type DAC, with a suitable diagram. (7)

OR

X. (a) Design a PLA for implementing the following logic functions.

(1) f1=X1X2+X1X3'+X1'X2'X3 (2) f2=X1X2+X1'X2'X3+X1X3 (10)

(b) Explain the following for a DAC (1) Accuracy (2) Monotonicity. (5)
